

BLOCK PROCESSING IN A MAXIMUM A POSTERIORI PROCESSOR FOR REDUCED POWER CONSUMPTION

ABSTRACT OF THE DISCLOSURE

5 A maximum *a posteriori* (MAP) processor employs a block processing technique for the
MAP algorithm to provide a parallel architecture that allows for multiple word memory
read/write processing and voltage scaling of a given circuit implementation. The block
processing technique forms a merged trellis with states having modified branch inputs to provide
the parallel structure. When block processing occurs, the trellis may be modified to show
10 transitions from the oldest state at time $k-N$ to the present state at time k . For the merged trellis,
the number of states remains the same, but each state receives 2^N input transitions instead of the
two input transitions. Branch metrics associated with the transitions in the merged trellis are
cumulative, and are employed for the update process of forward and backward probabilities by
the MAP algorithm. During the update process, the read/write operation for an implementation
15 transfers N words of length N for each update operation, but the frequency (and hence, number)
of update operations is reduced by a factor of N . Such voltage scaling and multiple word
memory read/write may provide reduced power consumption for a given implementation of MAP
processor in, for example, a DSP.